02/17/2004 16:50 9497844601

Attorney Docket No.: 0180163 Serial No.: 10/010,280

<u>REMARKS</u>

The present amendment is in response to the Office Action, dated November 29, 2002, where the Examiner has *finally rejected* claims 1, 10, 15 and 16 pending in the application.

Claim 22-27 have been allowed, and claims 2-9 and 11-14 have been objected to. By the present amendment, claims 1 and 10 have been amended. Accordingly, claims 1-16 and 22-27 are pending in the application. Reconsideration and allowance of pending claims 1-16 and 22-27 in view of the amendments and the following remarks are respectfully requested.

A. New Title

As requested by the Examiner, applicant has amended the title to correct a typographical error. Accordingly, the new title now recites "Pretreatment of ONO Layer For Flash Memory."

Applicant respectfully submits that typographical error in the title has now been corrected.

B. Rejection of Claims 1, 10, 15 and 16 Under 35 USC § 103(a)

The Examiner has rejected claims 1, 10, 15 and 16 under 35 USC § 103(a) as being unpatentable over Hong et al. (USPN 5,445,984) ("Hong '984") in view of Eitan (USPN 5,966,603) ("Eitan '603"). Applicant respectfully disagrees; however, in order to expedite the prosecution of this application, applicant has amended independent claims 1 and 10 to specify "pretreating the silicon nitride layer, said pretreating including oxidizing the silicon nitride layer, wherein a thickness of the silicon nitride is altered by no more than 10 to 20 Angstroms" and "forming a second layer of silicon dioxide on the pretreated silicon nitride layer by deposition." For the reasons that follow, applicant submits that amended independent claims 1 and 10 are patentably distinguishable over the cited art of record, considered either solely or in combination.

Independent claims 1 and 10 are directed to a method for forming a dielectric structure and a polysilicon structure, respectively, each of which comprises a first silicon dioxide layer, a

Attorney Docket No.: 0180163 Serial No.: 10/010,280

silicon nitride layer and a second silicon dioxide layer, i.e., an "ONO" structure. As recited by amended claims 1 and 10, the method includes "pretreating the silicon nitride layer, said pretreating including oxidizing the silicon nitride layer, wherein a thickness of the silicon nitride is altered by no more than 10 to 20 Angstroms." The method further includes forming a second layer of silicon dioxide on the pretreated silicon nitride layer by deposition.

It is noted at the outset, that the cited references, Hong '984 and Eitan '603, neither disclose nor suggest "pretreating" the silicon nitride layer. Specifically, the Examiner acknowledges that Hong '984 fails to teach deposition of the second silicon oxide layer after oxidizing the silicon nitride layer (Page 4 of the Detailed Action). Likewise, the Eitan '603 reference is devoid of any teaching or suggestion to pretreat the silicon nitride layer. However, the Examiner cites Eitan '603 as disclosing teaching the formation of the top oxide layer 34 by a combination of oxidation and deposition (Page 5 and 6 of the Detailed Action).

The Eitan '603 approach for forming the top oxide layer 34, however, is a significant departure from pretreating silicon nitride layer and subsequently forming the second silicon oxide layer as specified in claims 1 and 10. In Eitan '603, oxidation of the nitride layer involves a substantial consumption of the nitride layer itself. For example, Eitan '603 discloses that half of the oxide thickness of the top oxide layer "comes from the consumed nitride" (Col 3:54-57). In contrast, pretreatment as recited in claims 1 and 10 involved merely altering the nitride layer "by no more than 10 to 20 Angstroms." Moreover, in Eitan '603, formation of the top oxide layer 34 involves the oxidation of the nitride layer in Eitan '603 to form part of the top oxide layer 34. It is for this reason that a substantial portion of the nitride layer is consumed in Eitan '603. In contrast, the pretreating step as recited in claims 1 and 10 merely alter the nitride layer, so that, for example, the mobile ionic contaminants in the nitride layer is reduced. In other words, the oxidation process in Eitan '603 is part of the formation of the top oxide, whereas in claims 1 and

Attorney Docket No.: 0180163 Serial No.: 10/010,280

and 10 specify that formation of the second silicon oxide layer is carried out by deposition, not by oxidation nor by a combination of oxidation and deposition. In sum, if oxidation of the nitride layer is carried out as disclosed by Eitan '603, such a process would not involve pretreatment of the nitride layer as specified in claims 1 and 10, but rather the consumption of the nitride layer to form a significant portion of the top oxide layer. Therefore, the combined teaching of Hong '984 and Eitan '603 fail to disclose, teach or suggest the claimed invention as recited in claims 1 and 10. Accordingly, it is respectfully submitted that rejection of independent claim 1 and its corresponding dependent claims 2-9, and independent claim 10 and its corresponding dependent claims 11-16 have been traversed, and that therefore claims 1-16 should now be allowed.

C. Objection to Claims 2, 6 and 11-14 Under 37 CFR § 1.75

The Examiner has objected to claims 2, 6 and 11-14 under 37 CFR § 1.75 as being substantial duplicates of claims 22-27, respectively. As discussed above independent claims 1 and 10 have been amended. Applicant respectfully submits that dependent claims 2 and 6 depending from independent claim 1 and dependent claims 11-14 depending from independent claim 10, due to the amendments to claims 1 and 10, are not substantial duplicates of claims 22-27, respectively. For the reasons discussed above in conjunction with claims 1 and 10, applicant respectfully submits that claims 2, 6 and 11-14 should now be allowed.

D. Allowed Claims

Claims 22-27 stand allowed.

Attorney Docket No.: 0180163 Serial No.: 10/010,280

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The title has been amended as follows:

Oxidizing Pretreatment of NON Of ONO Layer For Flash Memory

In the Claims:

Claims 1 and 10 have been amended as follows:

1. (Twice Amended) A method of forming a dielectric structure for a flash memory cell, the method comprising:

forming a first layer of silicon dioxide overlying a gate electrode of the flash memory cell;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing pretreating the silicon nitride layer, said pretreating including oxidizing the silicon nitride layer, wherein a thickness of the silicon nitride is altered by no more than 10 to 20 Angstroms; and

forming depositing a second layer of silicon dioxide on the pretreated silicon nitride layer by deposition after the oxidizing.

10. (Twice Amended) A method of making a flash memory cell including a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer; forming a silicon nitride layer on the first layer of silicon dioxide;

Attorney Docket No.: 0180163

Serial No.: 10/010,280

oxidizing pretreating the silicon nitride layer, said pretreating including oxidizing the silicon nitride layer, wherein a thickness of the silicon nitride is altered by no more than 10 to 20 Angstroms; and

forming depositing a second layer of silicon dioxide on the pretreated silicon nitride layer by deposition after the exidizing.

Attorney Docket No.: 0180163

Serial No.: 10/010,280

E. Conclusion

For all the foregoing reasons, allowance of claims 1-16 and 22-27 pending in the present application is respectfully requested.

> Respectfully Submitted; FARJAMI & FARJAMI LLP

Michael Farjami, Esq. Reg. No. 38,135

Michael Farjami, Esq. FARJAMI & FARJAMI LLP 16148 Sand Canyon Irvine, California 92618

Tel: (949) 784-4600 Fax: (949) 784-4601

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service "First Class Mail Post Office to addressee" Service under 37 C.F.R. Sec. 1.10 addressed to Assistant Commissioner for Patents, Washington, D.C. 2023 I, on 2 11 03.